



# High-Rate Ka-Band Modulator for the NISAR Mission

Michael Pugh,  
Igor Kuperman, Michael Kobayashi, Fernando Aguirre,  
Michael Kilzer, Carl Spurgers

Jet Propulsion Laboratory, California Institute of Technology  
Presented at IEEE Aerospace Conference in Big Sky, Montana  
March 2018



# Agenda

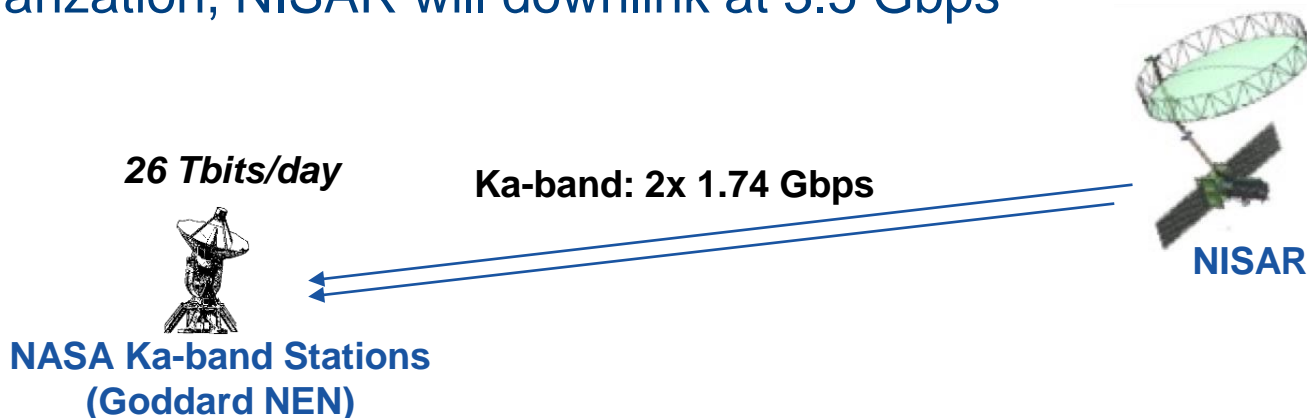
- NISAR Mission
- UST-KaM Comm Architecture
- UST-KaM Specs
- UST Radio Family
- UST-KaM Heritage
- UST-KaM Hardware Architecture
- Digital Processor Module
- Power Supply Module
- Ka-band Transmit Module
- EM Test Results
- Future Plans



Jet Propulsion Laboratory  
California Institute of Technology

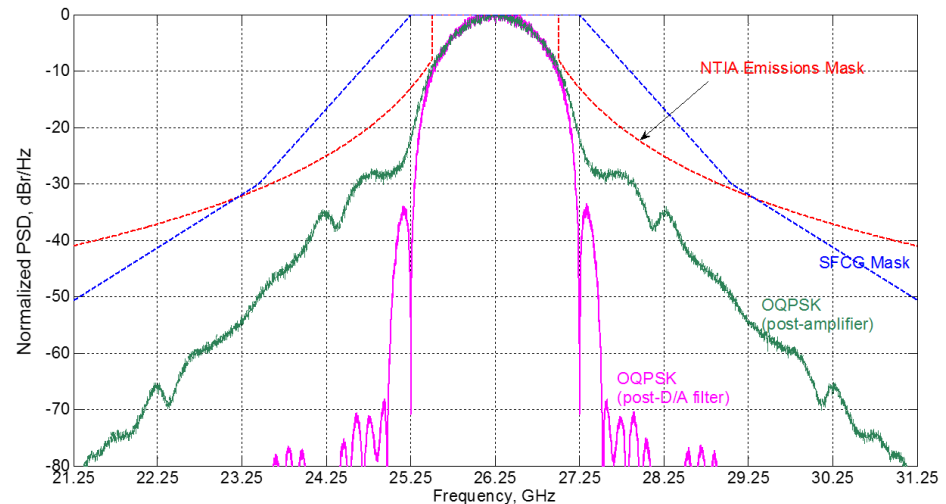
# NISAR Mission

- The NASA ISRO Synthetic Aperture Radar (NISAR) will use dual-band SAR to study the dynamics of ice flow, crust deformation, and landscape change in unprecedented detail
- To achieve this, NISAR will produce massive data volumes (>26 Tbits per day) and require Gbps-class downlinks
- With no commercially available flight transmitters capable of >1 Gbps and at an acceptable NASA Technology Readiness Level (TRL), JPL has developed the Universal Space Transponder – Ka-band Modulator (UST-KaM)
- Utilizing two UST-KaM units transmitting 1.74 Gbps on each polarization, NISAR will downlink at 3.5 Gbps



# UST-KaM Communication Architecture

- UST-KaM transmits 2 Gbps coded data rate while complying with the NTIA 1.5 GHz band allocation for near-Earth Ka-band (25.5-27 GHz)
- Offset-QPSK modulation with baseband filtering
  - 1 GHz RF low-pass filters on I/Q as well as RRC digital pulse shaping
  - Bandwidth efficient while still offering good  $E_b/N_0$  performance
  - Offset I and Q transitions is resilient to spectral regrowth by saturated amplifiers
- CCSDS LDPC 7/8 encoding
  - High-rate code minimizes overhead while still providing ~8 dB of coding gain
  - Synchronizes with CCSDS AOS framing, sharing single sync marker
  - Pseudo-randomizer to ensure bit transition density



Simulated Spectrum of Filtered OQPSK pre- and post- Saturated Amp

# UST-KaM Specs

## TX Specs

Frequencies	Ka-band (25.5-27 GHz)
Bandwidth	< 1.5 GHz
Coded Data Rates	500, 1000, 2000 Gbps
Modulations	QPSK / OQPSK with Custom Baseband Analog Filtering
Digital Pulse Shaping	Root Raised Cosine (Optional)
Channel Coding	LDPC with Rate 223/255 (~7/8)
RF Output Power	+12 dBm

## Environmental Specs

Flight Allowable Temperatures	-20° to +50° C
Mechanical Environments	>15 grms Random Vibration >2000 g Shock
Radiation	50 krad



## Interface Specs

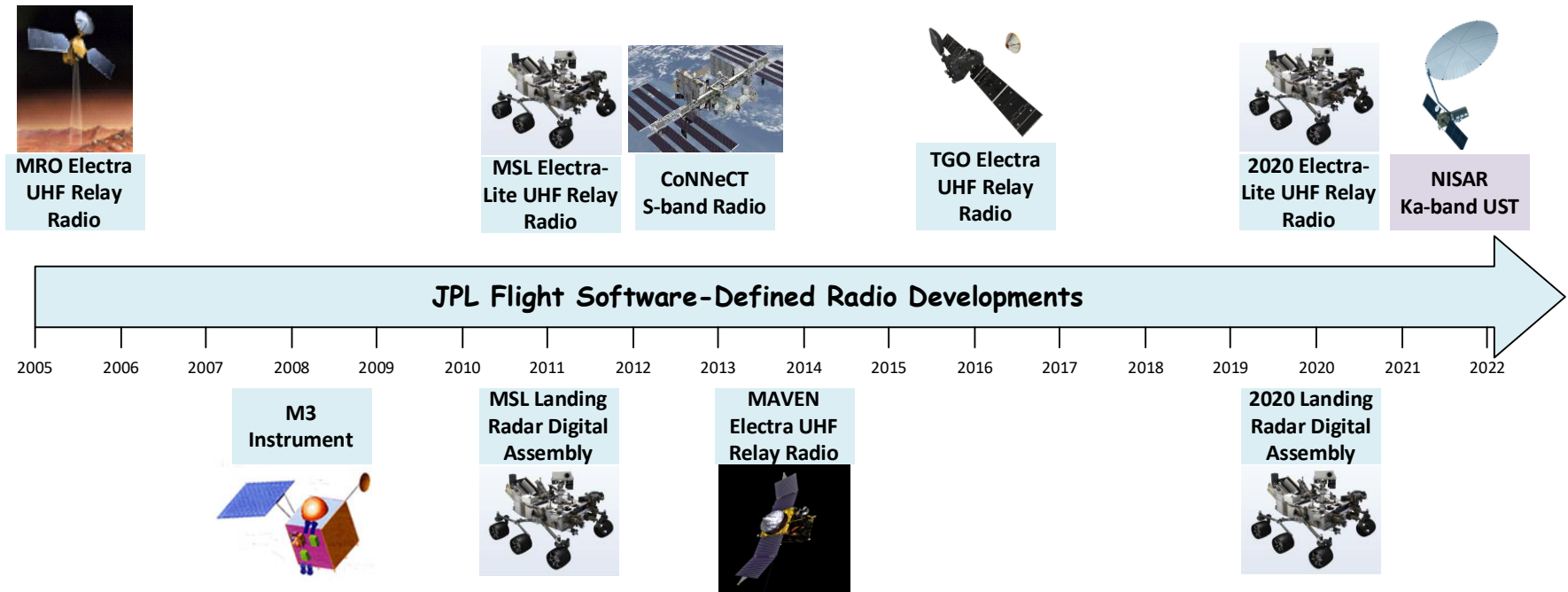
Mass	4.5 kg
Power Consumption	40 W TX Mode 20 W Standby Mode
Cmd/Tlm Interface	1553, RS-422, or Spacewire
High Speed Data Interface	TLK WizardLink SERDES (up to 2 Gbps)
Power Interface	22-36 V Unregulated Bus
Dimensions	25 x 20 x 11 cm (L x W x H)

# Universal Space Transponder Radio Family

- The high-rate Ka-band Modulator developed as part of JPL's Universal Space Transponder (UST) product line
- UST is JPL's next generation software defined radio family, designed to meet the following goals:
  - Modular hardware and digital architectures that provide flexibility to meet a large variety of telecom, navigation, and radio science needs with a single radio platform
  - Expandability to handle multiple RF links (UHF, S-, X-, or Ka-band), allowing a single unit to support both relay and direct-to-Earth communications for near-Earth or deep space missions
  - Significantly higher bi-directional data rates than current deep-space radios to increase mission return data volumes
  - Sufficient digital resources to enable advanced modulations, FEC coding, protocols, and navigation techniques
  - In-flight reprogrammable to allow new functionality or bug fixes during any mission phase
  - Frequency agility to increase flexibility in channel assignments or to avoid EMI

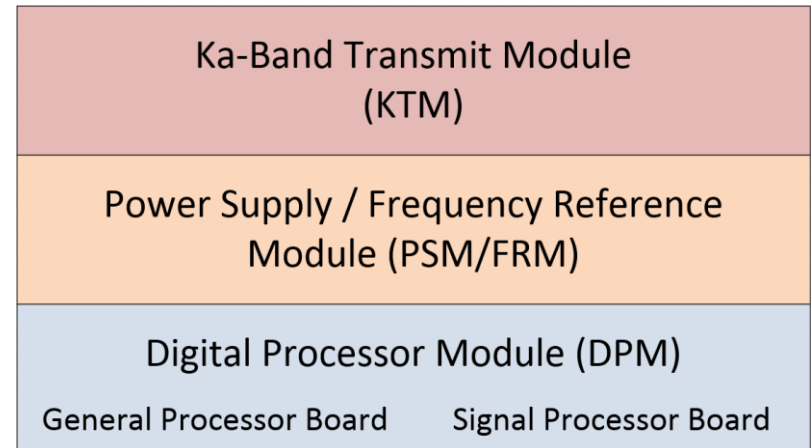
# UST-KaM Heritage

- UST-KaM leverages design features from JPL's previous flight SDRs
  - Stacked module configuration with separate digital, power, and RF modules
  - One-time programmable Housekeeper FPGA and PROM for reliable Safe Mode
  - Xilinx FPGA with in-flight reprogrammable firmware for modem processing
  - SPARC microprocessor with in-flight reprogrammable Application Software



# UST-KaM Hardware Architecture

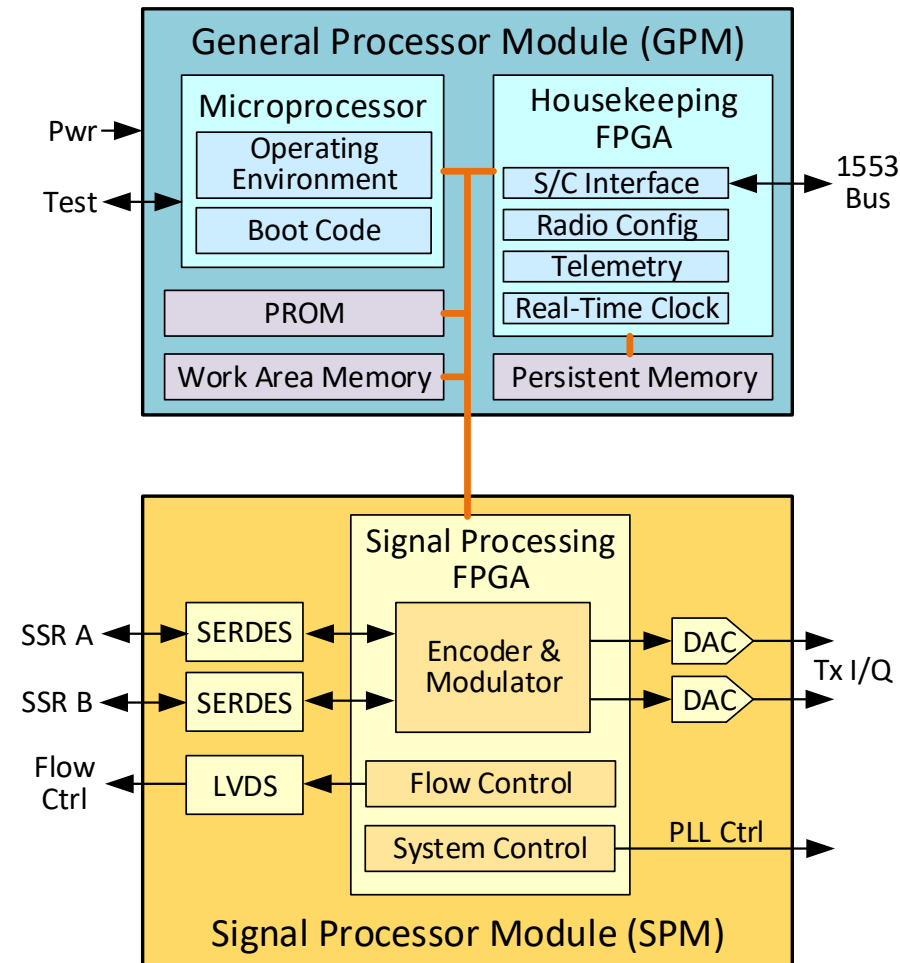
- UST KaM uses a modular architecture with three modules or “slices” that are connected by coax cables and a single flex harness in a rear raceway
- The bottom digital and power modules are common to any UST variant, with the needed RF modules stacked on top
- Ka-Band Transmitter Module (KTM)
  - Modulates I/Q baseband signals onto Ka-band RF transmission
  - Provides 2 GHz reference for DACs in DPM
- Power Supply / Frequency Reference Module (PSM/FRM)
  - Converts primary power to regulated secondary voltages
  - Provides TCXO frequency reference to other modules
- Digital Processor Module (DPM)
  - Provides all the digital interfaces with the spacecraft
  - Performs baseband processing and modulation of transmit data
  - Unit housekeeping functions and telemetry collection

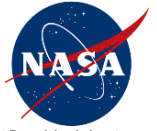




# Digital Processor Module (DPM) Architecture

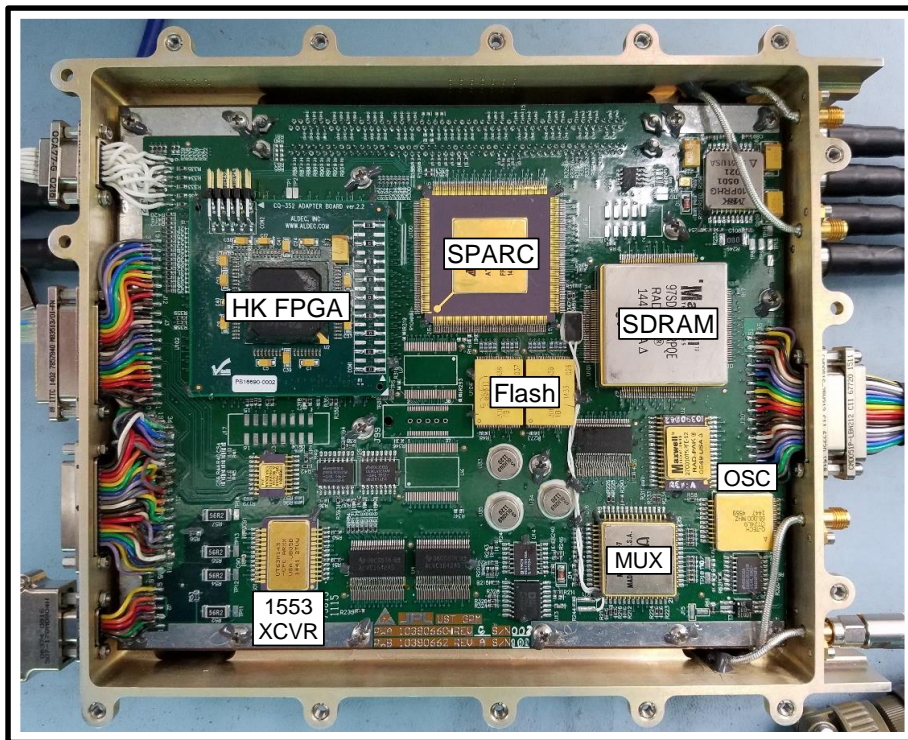
- Compliant with NASA Space Telecom Radio System (STRS) standard for software defined radios
- General Processor Module (GPM)
  - Command and telemetry over MIL-STD-1553B, RS-422, or Spacewire interface
  - Analog telemetry collection (voltages, temperatures, etc.)
  - Provides storage and management of software and firmware images for all reprogrammable DPM elements
  - Configuration and scrubbing interface for Xilinx Virtex-5 FPGA on SPM
  - Overall radio management, including PSM and RF module control
- Signal Processor Module (SPM)
  - High-speed interfaces to Spacecraft SSR via TLK2711 SERDES transceivers
  - Virtex-5 FPGA for modem processing
  - In-flight reprogrammable
  - High-speed DACs for I/Q data
  - TX frequency synthesizer programming





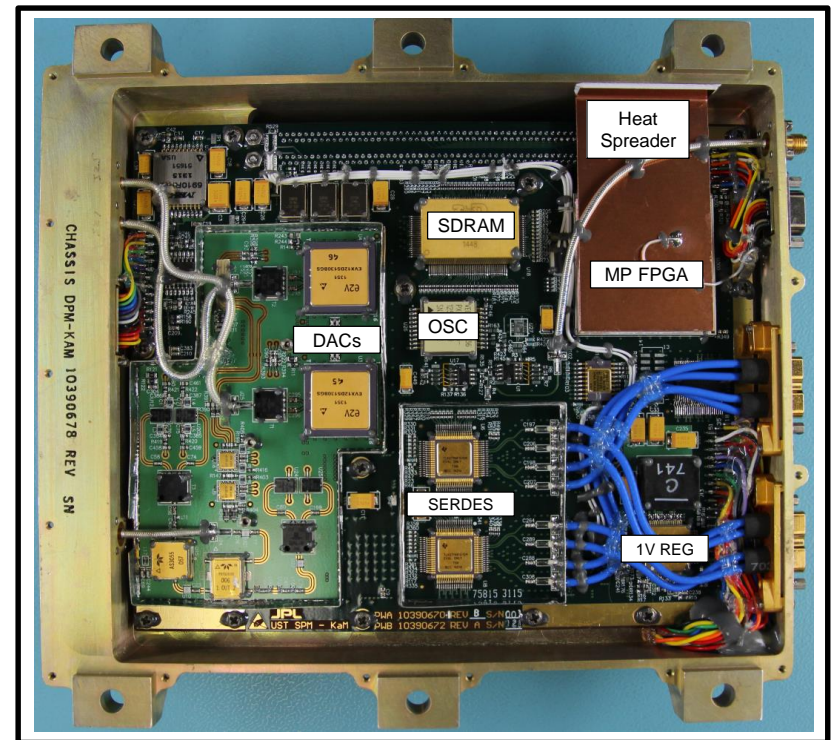
# DPM Details

- Top side of the DPM
  - Housekeeper RTAX FPGA
  - SPARC Microprocessor with SDRAM runtime memory and flash for SW/FW storage
  - 1553 and SpaceWire/RS-422 interfaces
  - Analog MUX and telemetry ADC
  - PSM and RF module control outputs



EM DPM Slice Top (GPM PWA Side)

- Bottom side of the DPM
  - Xilinx Virtex-5 Modem Processor FPGA
  - Xilinx power sequencing/distribution
  - High-speed Transmit I/Q DACs
  - SSR SERDES transceivers
  - SDRAM buffer memory

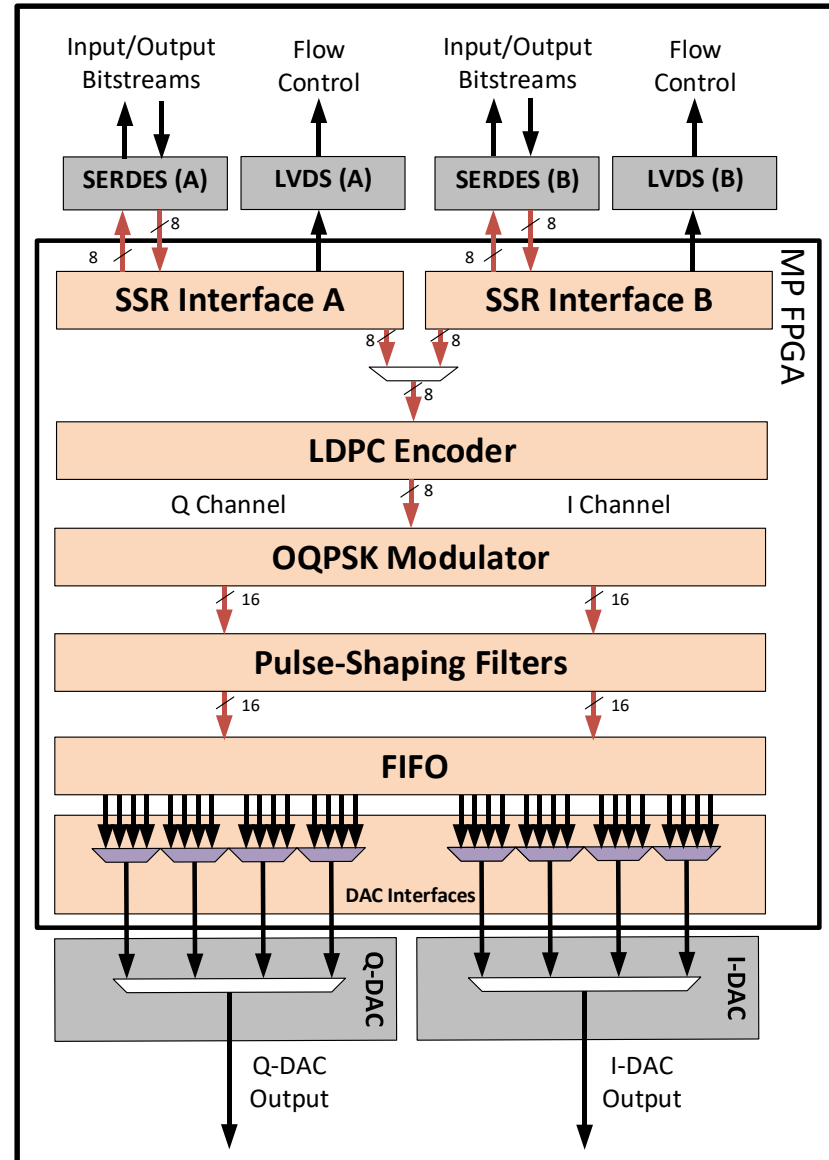


EM DPM Slice Bottom (SPM PWA Side)



# Modem Processor FPGA

- All DSP implemented in Xilinx Virtex-5 Modem Processor (MP) FPGA
- High-speed processing with 125 MHz main clock
- 2 Gbps, 16-bit parallel SSR interface with 8b/10b encoding and K-codes for AOS frame synchronization
- Parallel CCSDS (860,7136) low-density parity check (LDPC-7/8) encoder with pseudorandomizer and ASM attachment
- Parallel 16-bit OQPSK I/Q modulator with 2 complex samples per channel symbol at 2 Gbps
- Parallel Root-Raised Cosine (RRC) pulse-shaping filter for inter-symbol interference (ISI) reduction
- High-speed interface logic to 12-bit DACs with built-in 4:1 multiplexer



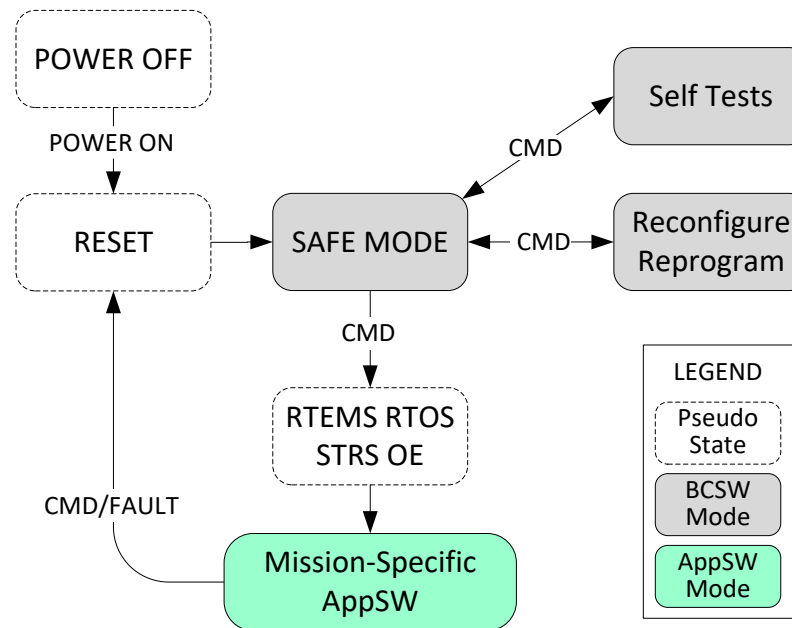
# Software

Boot Code Software (BCSW) provides a “Safe Mode” – always available and loaded on power-on or reset from one-time programmable rad-hard PROM

- Telemetry collection and reporting
- Command and control via 1553
- Basic commands for AppSW loading
- Accepts new FW/SW images over 1553 and manages flash storage

Application Software (AppSW) provides mission-specific functionalities on top of basic BCSW functions – loaded from image in flash memory

- Programs and initializes the Modem Processor FPGA and configures modem parameters
- Configures DACs, memories, and SSR data interfaces
- Real-time amplitude adjustments to compensate for temperature variations

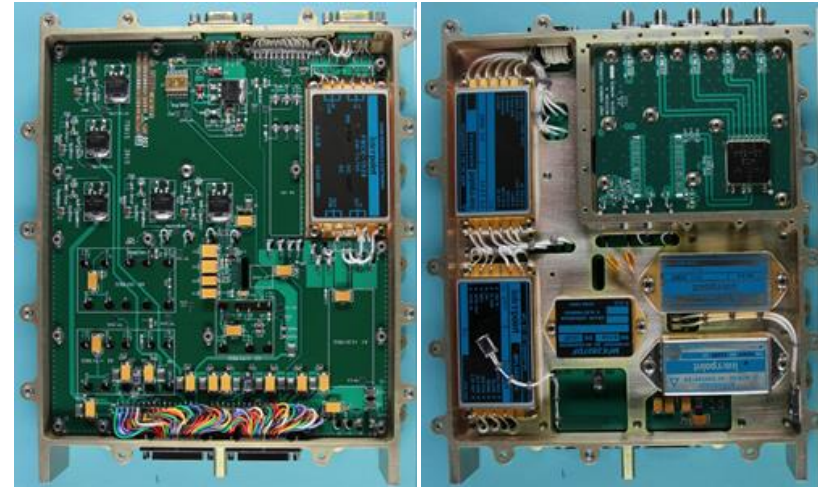
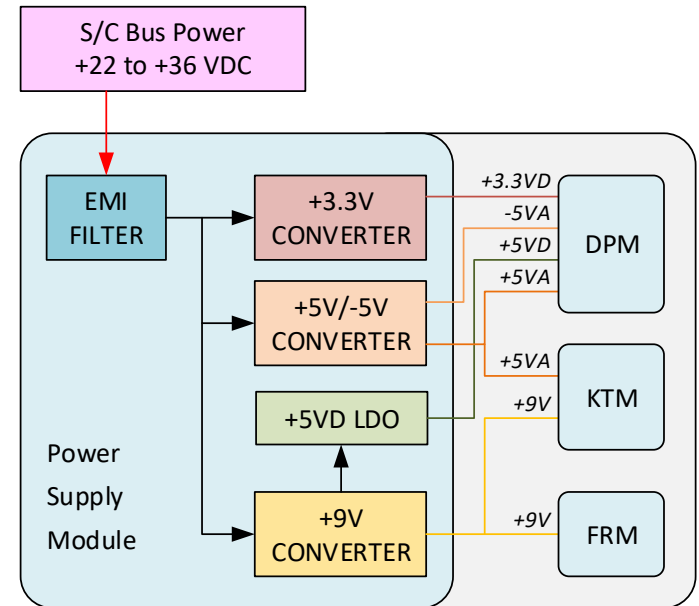






# Power Supply Module (PSM)

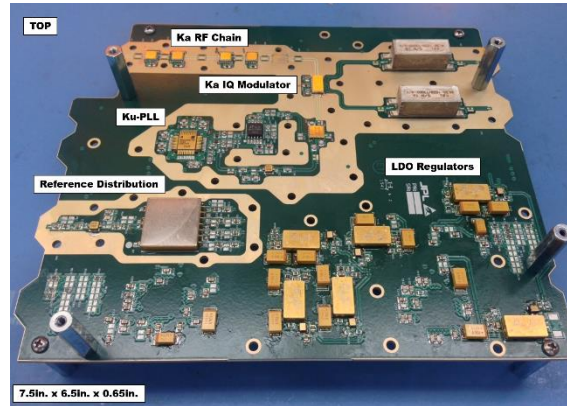
- Accepts unregulated 22 to 36V bus power input from Spacecraft
- Provides regulated secondary DC power to other UST modules
- Design is based on a heritage architecture, with the spacecraft power bus passing through an EMI filter and then distributing to various DC/DC secondary converters
- Additional PWB in dedicated cavity for TCXO frequency reference distribution
- Split chassis design with DC/DC converters and the frequency reference PWB on one side of a common floor and the power PWB on the other side



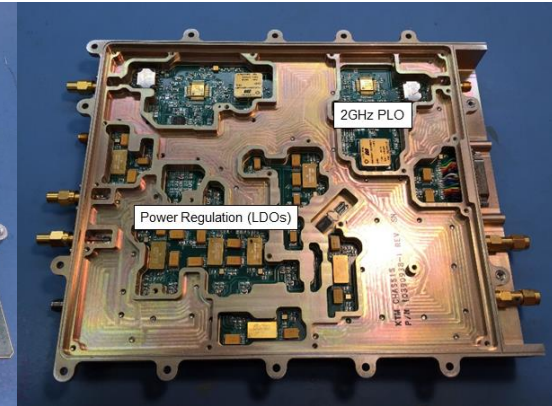


# Ka-Band Transmitter Module (KTM)

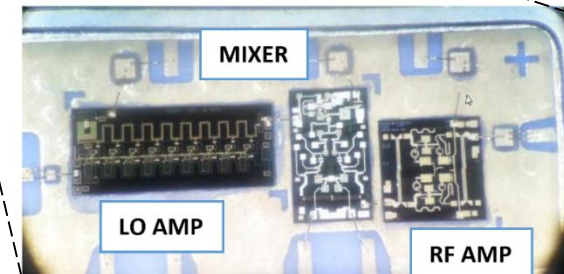
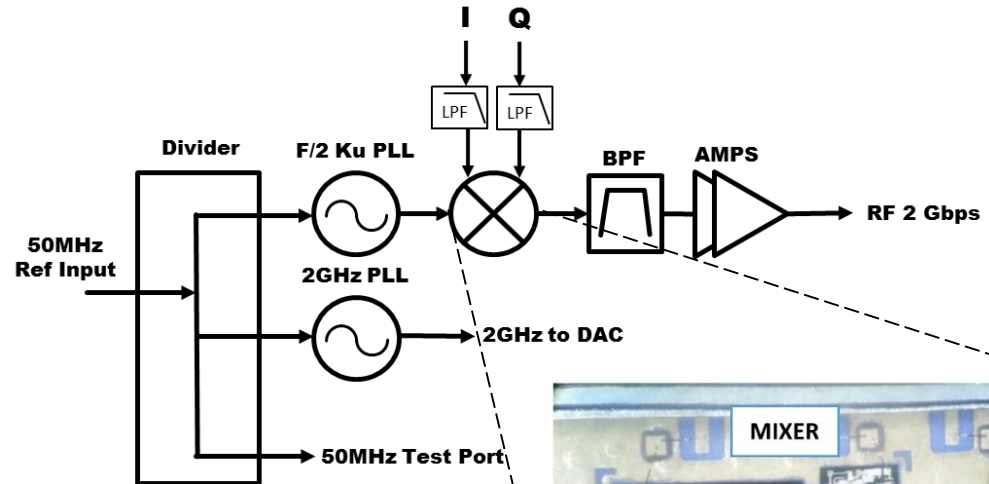
- Ka-band output carrier modulated by in-phase and quadrature (IQ) digital waveforms from the DPM
- Custom multi-chip module (MCM) sub-harmonic IQ modulator eliminates need for Ka-band VCO
- Analog baseband filtering for data side-lobe rejection
- Transmit output filtering for harmonics suppression
- On-board frequency synthesizers for DPM high-speed clock and KTM modulator LO
- All surface-mount technology (SMT) hybrids for package-size reduction and lower Ka-band interconnect losses
- Internal clamshell covers to reduce signal crosstalk



Ka-band Transmitter EM PWA  
(Top View)



Ka-band Transmitter EM  
Assembly (Bottom View)



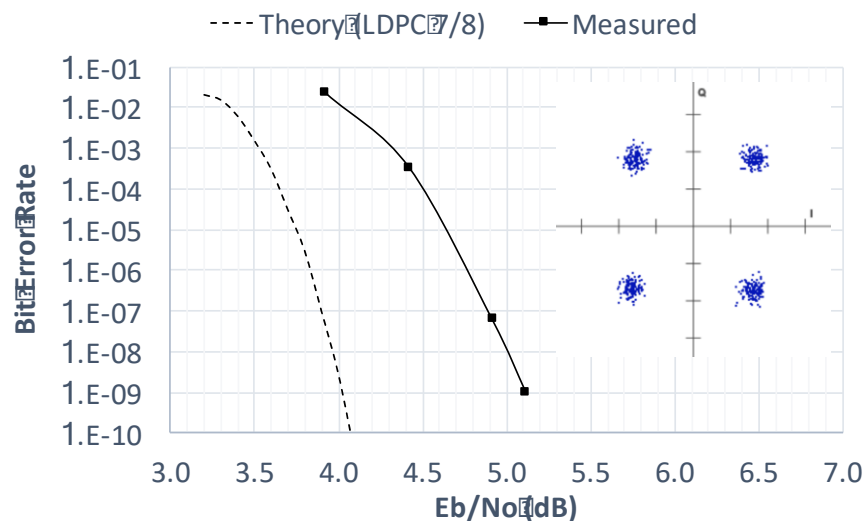
Custom MCM IQ Modulator



# Engineering Model Test Results

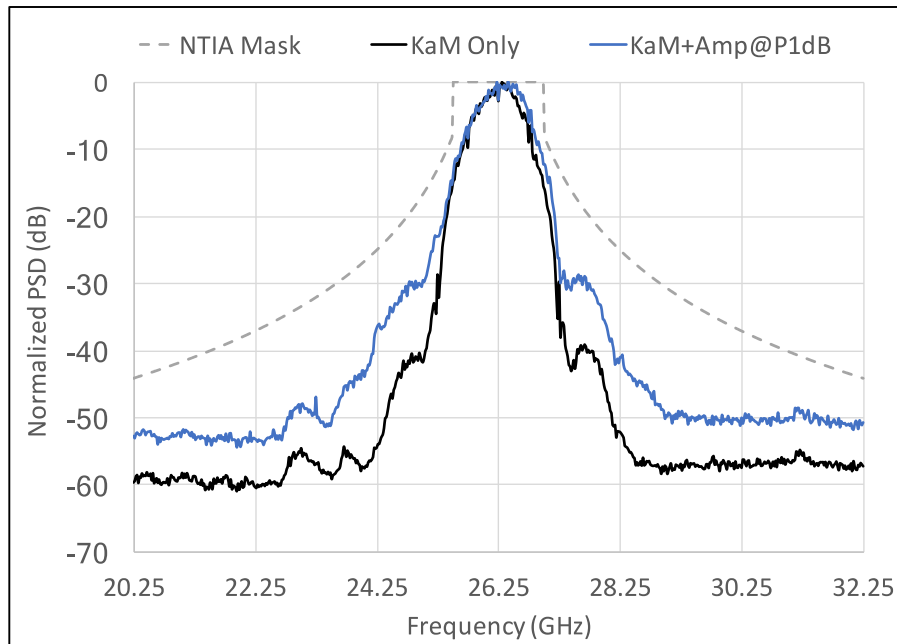
- NASA TRL 6 demonstrated via testing an engineering model in 2016, including three-axis dynamics, thermal vacuum, and EMI/EMC testing
- All specification met across the allowable flight temperature range
- Compatibility demonstrated with commercial, high-rate ground-station receivers from Zodiac and ViaSat

Parameter	Units	Spec.	Meas.
DC Power Consumption (Transmit Mode)	Watts	< 50.0	40.9
DC Power Consumption (Standby Mode)	Watts	< 24.0	19.9
RF Output Power	dBm	> 12.0	12.4
Carrier Frequency	GHz	26.25	26.25
Carrier Phase Noise (1 kHz – 10 MHz)	deg, rms	< 3.6	3.1
Coded Data Rate	Gbps	2.0	2.0
Phase Imbalance	deg	< 5.2	3.5
Amplitude Imbalance	dB	< 1.1	0.4
Spurious Outputs	dBc	< -60	None

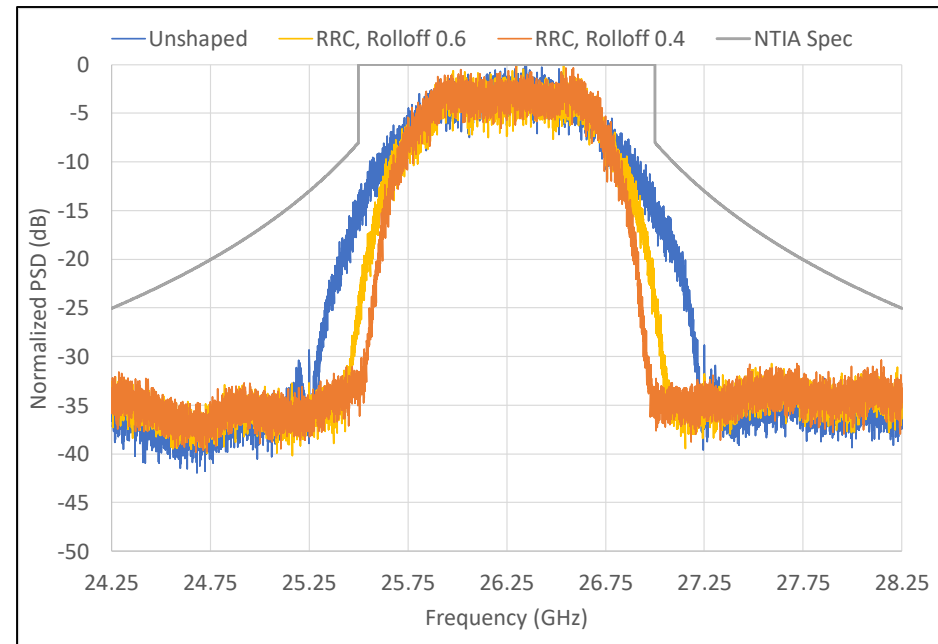


# Spectral Compliance and Pulse Shaping

- Consistent with simulations, NTIA compliance was maintained with a saturated, external RF amplifier
- Additional testing with RRC pulse shaping produced improved spectral efficiency for cases without significant saturation



Measured Spectrum pre- and post- Saturated Amp



Measured Spectrum with Digital Pulse Shaping



# Future Plans

- The NISAR project is currently in the flight hardware build phase with a scheduled launch for late 2020
  - Three flight models of the UST-KaM are currently being assembled at JPL
  - Flight models will be integrated in 2018 and complete a proto-flight qualification program in 2019
  - JPL will likely select and work with an industry partner on builds for any future missions
- Additional development planned for higher-rate UST-KaM operational modes to achieve ~4 Gbps transmission rate per unit
  - Operating dual SERDES inputs simultaneously for faster transfer from SSR
  - Higher-order modulations such as 16-APSK could increase data throughput at the cost of link SNR
  - Increasing channel symbol rate to 1.3 Gbps with RRC pulse shaping to maintain spectral compliance

# Acknowledgements

We would like to thank the following people for their contributions to the UST-KaM development:

Scot Stride, Susan Clancy, Anusha Yarlagadda, Kris Angkasa, Steve Allen, Sarah Holmes, Dave Orozco, Kirk Fleming, Thanh Tran, Josh Ravich, Kevin Hischer, John Koenig, Ray Quintero, Vachik Garkanian, Tuyen Ly, Carlos Esproles, Rich Rebele, Brian Custodero, Dave Bell, Charles Dunn, Larry Epp, and Dimitrios Antsos



Jet Propulsion Laboratory  
California Institute of Technology



**Jet Propulsion Laboratory**  
California Institute of Technology